

# ABSTRACT OF THE DISCLOSURE

1 A synchronous memory device and methods of operation and  
2 controlling such a device. The synchronous memory device includes  
3 input receiver circuitry to sample a first operation code synchronously  
4 with respect to an external clock signal. The synchronous memory  
5 device also includes a programmable register to store a binary value in  
6 response to the first operation code, wherein the binary value is  
7 representative of an amount of time to transpire before the memory  
8 device outputs data. The synchronous memory device also includes  
9 output driver circuitry to output data in response to a second  
10 operation code and after the amount of time transpires. A first  
11 portion of data is output synchronously with respect to a first  
12 transition of the external clock signal and a second portion of data is  
13 output synchronously with respect to a second transition of the  
14 external clock signal.